

74F148

8-Line to 3-Line Priority Encoder

General Description

The 'F148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

- Provides 3-bit binary priority code
- Input enable capability
- Signals when data is present on any input
- Cascadable for priority encoding of n bits

Features

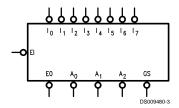
■ Encodes eight data lines in priority

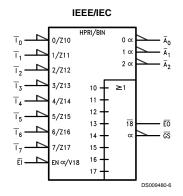
Ordering Code:

Commercial	Package	Package Description					
	Number						
74F148PC	N16E	16-Lead (0.300" Wide) Molded Dual-In-Line					
74F148SC (Note 1)	M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC					
74F148SJ (Note 1)	M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ					

Note 1: Devices also available in 13" reel. Use Suffix = SCX and SJX.

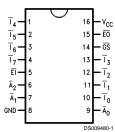
Logic Symbols





Connection Diagram

Pin Assignment for SOIC and DIP



Unit Loading/Fan Out

		74F				
Pin Names	Description	U.L.	Input I _{IH} /I _{IL}			
		HIGH/LOW	Output I _{OH} /I _{OL}			
Īo	Priority Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA			
Ī ₁ —Ī ₇	Priority Inputs (Active LOW)	1.0/2.0	20 μA/–1.2 mA			
ΕĪ	Enable Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA			
ĒΟ	Enable Output (Active LOW)	50/33.3	–1 mA/20 mA			
GS	Group Signal Output (Active LOW)	50/33.3	–1 mA/20 mA			
$\overline{A}_0 - \overline{A}_2$	Address Outputs (Active LOW)	50/33.3	–1 mA/20 mA			

Functional Description

The 'F148 8-input priority encoder accepts data from eight active LOW inputs $(\overline{l}_0-\overline{l}_7)$ and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input (\overline{EI}) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal output (\overline{GS}) and Enable Output (\overline{EO}) are provided along with the three priority data outputs $(\overline{A}_2,\overline{A}_1,\overline{A}_0)$. \overline{GS} is active LOW when any input is LOW: this indicates when any input is active. \overline{EO} is active LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows cascading for priority encoding on any number of input signals. Both \overline{EO} and \overline{GS} are in the inactive HIGH state when the Enable Input is HIGH.

Truth Table

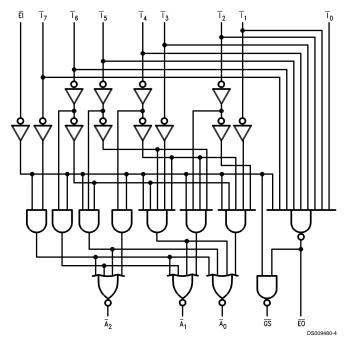
	Inputs						Outputs						
ΕĪ	Īο	Ī1	Ī ₂	Ī ₃	Ī ₄	Ī ₅	Ī ₆	Ī ₇	GS	Āo	\overline{A}_1	\overline{A}_{2}	ΕO
Н	Х	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Н	Н	Н	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Х	Χ	Χ	Χ	Χ	Χ	Χ	L	L	L	L	L	Н
L	Х	Χ	Χ	Χ	Χ	Χ	L	Н	L	Н	L	L	Н
L	Х	Χ	Χ	Χ	Χ	L	Н	Н	L	L	Н	L	Н
L	Х	Χ	Χ	Χ	L	Н	Н	Н	L	Н	Н	L	Н
L	Х	Χ	Χ	L	Н	Н	Н	Н	L	L	L	Н	Н
L	Х	Χ	L	Н	Н	Н	Н	Н	L	Н	L	Н	Н
L	Х	L	Н	Н	Н	Н	Н	Н	L	L	Н	Н	Н
L	L	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Storage Temperature -65°C to +150°C

Ambient Temperature under Bias -55°C to +125°C

Junction Temperature under Bias -55°C to +175°C

Plastic -55°C to +150°C

 $V_{\rm CC}$ Pin Potential to

Ground Pin -0.5V to +7.0V Input Voltage (Note 3) -0.5V to +7.0V Input Current (Note 3) -30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)

Current Applied to Output

in LOW State (Max) $\qquad \qquad \text{twice the rated I}_{\text{OL}} \text{ (mA)}$

Recommended Operating Conditions

Free Air Ambient Temperature

Commercial 0°C to +70°C

Supply Voltage

Commercial +4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these

conditions is not implied.

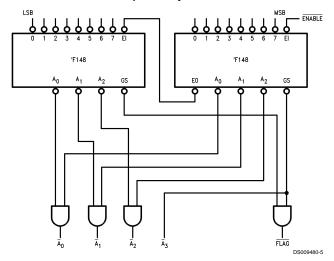
Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	bol Parameter		74F			Units	V _{cc}	Conditions	
			Min	Тур	Max				
V _{IH}	Input HIGH Voltage					V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Vo	oltage			-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH	74F 10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA	
	Voltage	74F 5% $V_{\rm CC}$	2.7					I _{OH} = -1 mA	
V _{OL}	Output LOW	74F 10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA	
	Voltage								
I _{IH}	Input HIGH	74F			5.0	μA	Max	V _{IN} = 2.7V	
	Current								
I _{BVI}	Input HIGH Current	74F			7.0	μA	Max	V _{IN} = 7.0V	
	Breakdown Test								
I _{CEX}	Output High	74F			50	μA	Max	V _{OUT} = V _{CC}	
	Leakage Current								
V _{ID}	Input Leakage	74F	4.75			V	0.0	I _{ID} = 1.9 μA	
	Test							All Other Pins Grounded	
I _{OD}	Output Leakage	74F			3.75	μA	0.0	V _{IOD} = 150 mV	
	Circuit Current							All Other Pins Grounded	
I _{IL}	Input LOW				-0.6	mA	Max	$V_{IN} = 0.5V (\overline{I}_0, \overline{EI})$	
	Current				-1.2	mA		$V_{IN} = 0.5V (\bar{l}_1 - \bar{l}_7)$	
I _{os}	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V	
I _{CCH}	Power Supply Curren	t			35	mA	Max	V _O = HIGH	
I _{CCL}	Power Supply Curren	t			35	mA	Max	V _O = LOW	

Application

16-Input Priority Encoder

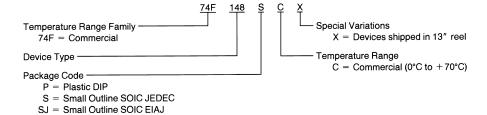


AC Electrical Characteristics

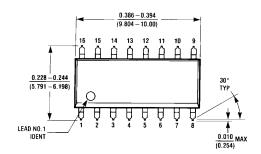
			74F		7	Units	
			T _A = +25°C		TA, VCC		
Symbol	Parameter		$V_{\rm CC}$ = +5.0V		C _L = 50 pF		
			$C_L = 50 pF$				
		Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	7.0	9.0	3.0	10.0	ns
t _{PHL}	\overline{I}_n to \overline{A}_n	3.0	8.0	10.5	3.0	12.0	
t _{PLH}	Propagation Delay	2.5	5.0	6.5	2.5	7.5	ns
t _{PHL}	\overline{I}_n to \overline{EO}	2.5	5.5	7.5	2.5	8.5	
t _{PLH}	Propagation Delay	2.5	7.0	9.0	2.5	10.0	ns
t _{PHL}	Ī _n to GS	2.5	6.0	8.0	2.5	9.0	
t _{PLH}	Propagation Delay	2.5	6.5	8.5	2.5	9.5	ns
t _{PHL}	\overline{EI} to \overline{A}_n	2.5	6.0	8.0	2.5	9.0	
t _{PLH}	Propagation Delay	2.5	5.0	7.0	2.5	8.0	ns
t _{PHL}	El to GS	2.5	6.0	7.5	2.5	8.5	
t _{PLH}	Propagation Delay	2.5	5.5	7.0	2.5	8.0	ns
t _{PHL}	El to EO	3.0	8.0	10.5	3.0	12.0	

Ordering Information

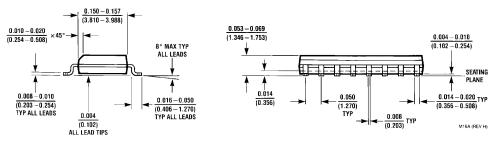
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



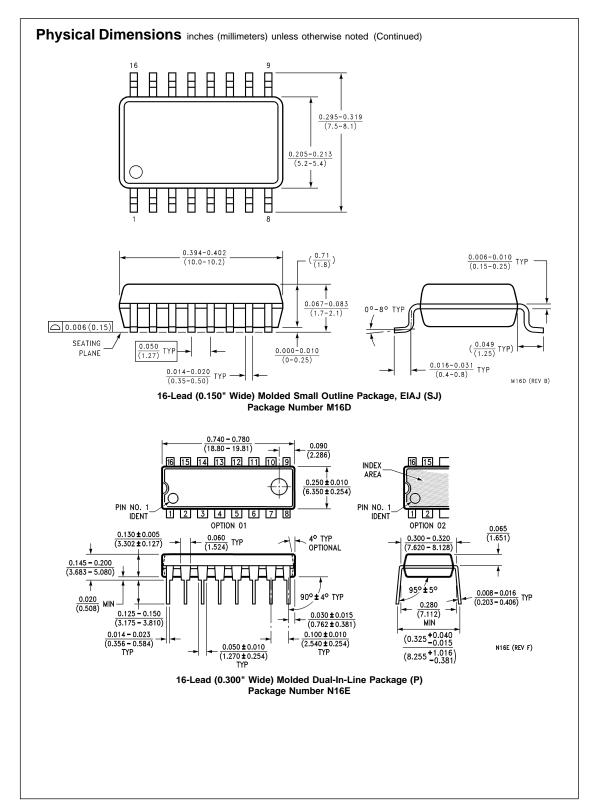
Physical Dimensions inches (millimeters) unless otherwise noted



DS009480-7



16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M16A



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