

MM54HC85/MM74HC85

4-Bit Magnitude Comparator

General Description

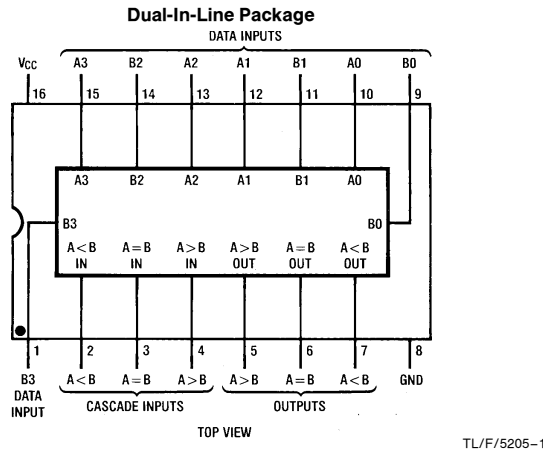
The MM54HC85/MM74HC85 is a 4-bit magnitude comparator that utilizes advanced silicon-gate CMOS technology. It is designed for high speed comparison of two four bit words. This circuit has eight comparison inputs, 4 for each word; three cascade inputs ($A < B$, $A > B$, $A = B$); and three decision outputs ($A < B$, $A > B$, $A = B$). The result of a comparison is indicated by a high level on one of the decision outputs. Thus it may be determined whether one word is "greater than," "less than," or "equal to" the other word. By connecting the outputs of the least significant stage to the cascade inputs of the next stage, words of greater than four bits can be compared. In addition the least significant stage must have a high level applied to the $A = B$ input, and a low level to the $A < B$, and $A > B$ inputs.

The comparator's outputs can drive 10 low power Schottky TTL (LS-TTL) equivalent loads, and is functionally, and pin equivalent to the 54LS85/74LS85. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 27 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram



Order Number MM54HC85 or MM74HC85

Truth Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	X	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			Units
				74HC $T_A = -40$ to $85^\circ C$		54HC $T_A = -55$ to $125^\circ C$	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	4.2	3.98	3.84	V
			6.0V	5.7	5.48	5.34	V
			6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	0.2	0.26	0.33	V
			6.0V	0.2	0.26	0.33	V
			6.0V	0.2	0.26	0.33	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15\text{ pF}$, $t_r = t_f = 6\text{ ns}$

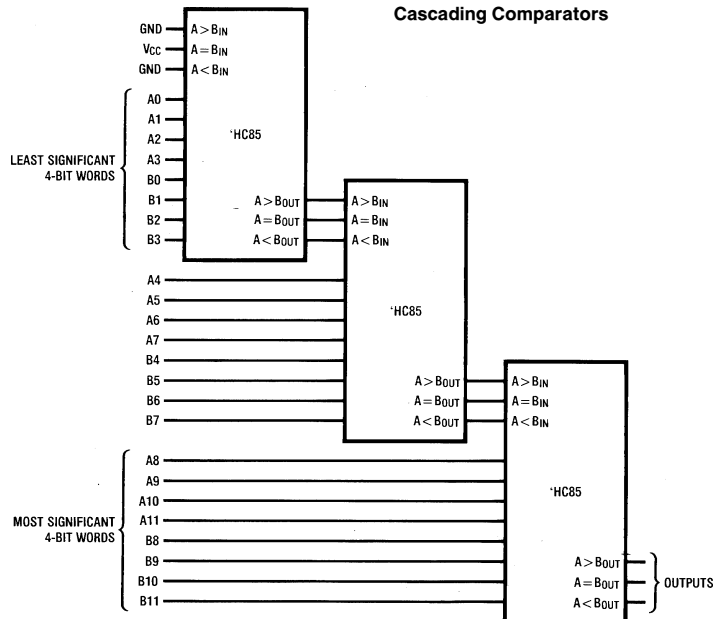
Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay Data Input to $A < B$ or $A > B$		20	36	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay $A = B$ Input to $A = B$ Output		12	20	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay Cascade Input to Output		13	26	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay Data Input to $A = B$		20	30	ns

AC Electrical Characteristics $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

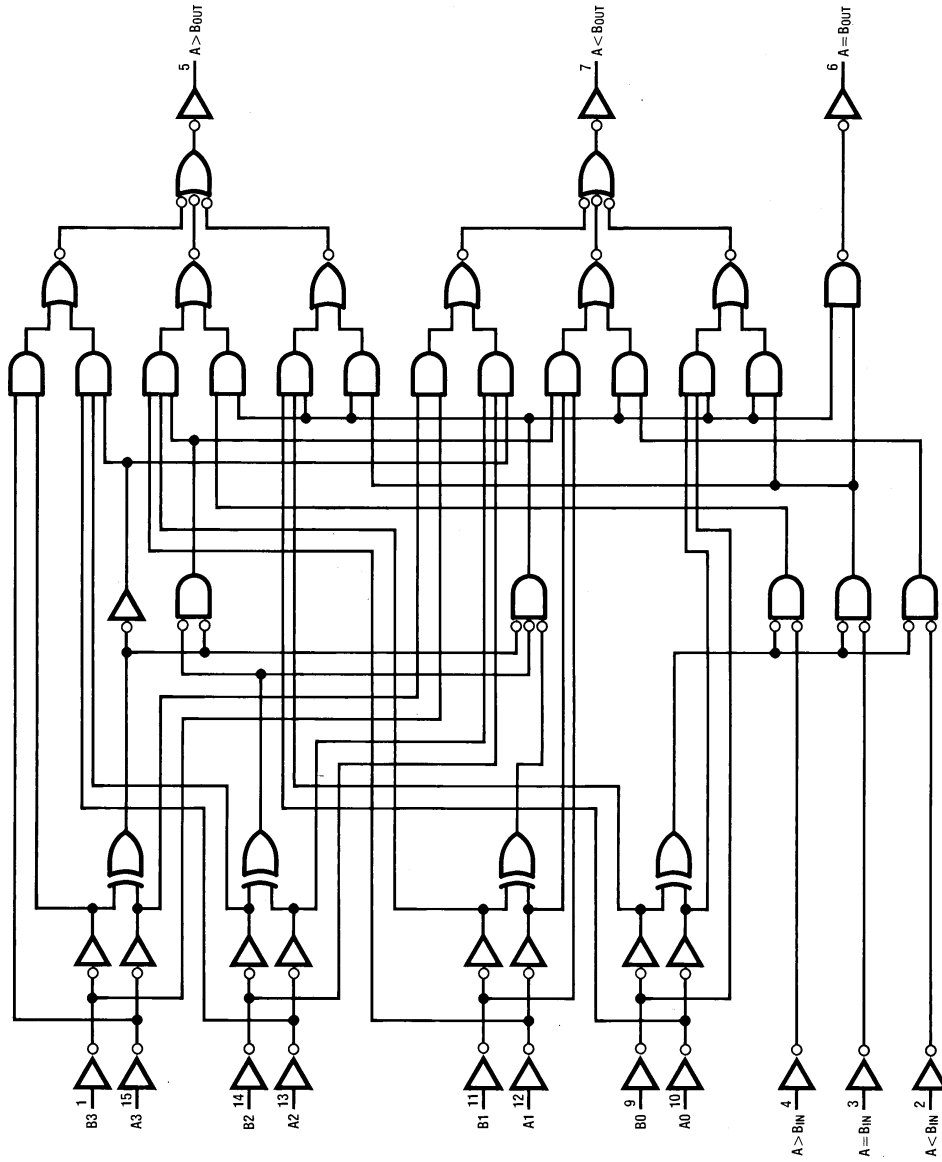
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		74HC	54HC	Units
				Typ		$T_A = -40\text{ to }85^\circ C$	$T_A = -55\text{ to }125^\circ C$	
t_{PHL} , t_{PLH}	Maximum Propagation Delay Data Input to Output		2.0V	100	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay Data Input to $A = B$ Output		2.0V	88	175	221	261	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay $A = B$ Input to $A = B$ Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay Cascade Input to Output (except $A = B$)		2.0V	70	155	195	231	ns
			4.5V	16	31	39	46	ns
			6.0V	13	26	33	39	ns
t_{TLH} , t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Typical Application



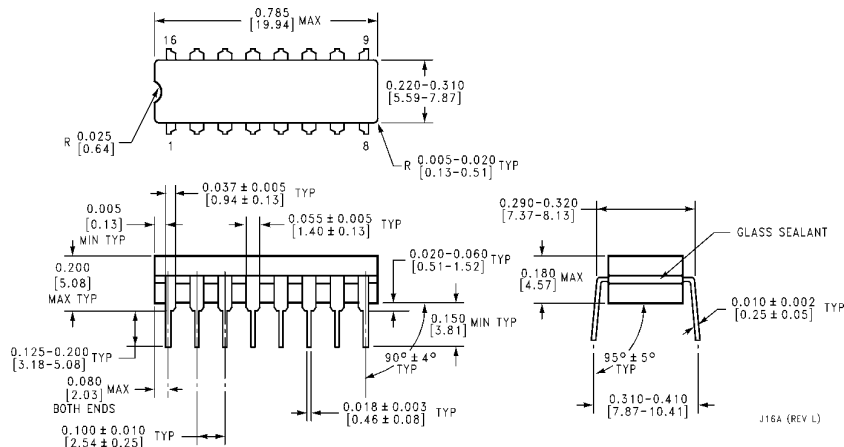
Logic Diagram



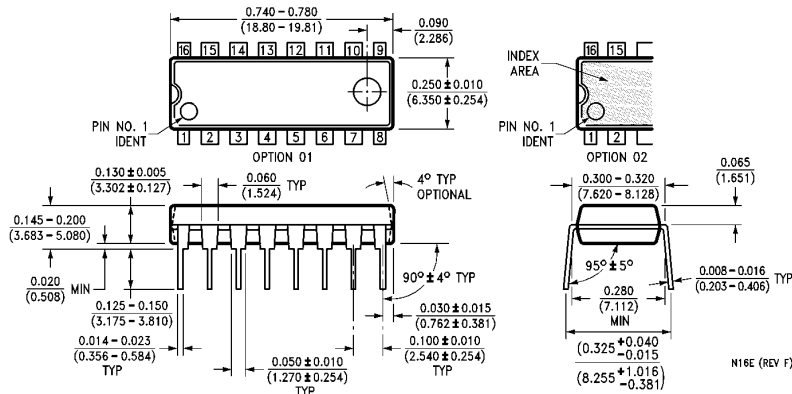
TL/F/5205-3



Physical Dimensions inches (millimeters)



Order Number MM54HC85J or MM74HC85J
NS Package J16A



Order Number MM74HC85N
NS Package N16E

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