National Semiconductor

February 1988

CD4510BM/CD4510BC BCD Up/Down Counter
CD4516BM/CD4516BC Binary Up/Down Counter

General Description

The CD4510BM/CD4510BC and CD4516BM/CD4516BC are monolithic CMOS up/down counters which count in BCD and binary, respectively.

The counters count up when the up/down input is at logical "1" and vice versa. A logical "1" preset enable signal allows information at the parallel inputs to preset the counters to any state synchronously with the clock. The counters are advanced one count at the positive-going edge of the clock if the carry in, preset enable, and reset inputs are at logical "0". Advancement is inhibited when any of these three inputs are at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" when the counter reaches its maximum count in the "up" mode or its minimum count in the "down" mode, provided the carry input is at logical "0" state. The counters are cleared asynchronously by applying a logical "1" voltage level at the reset input.

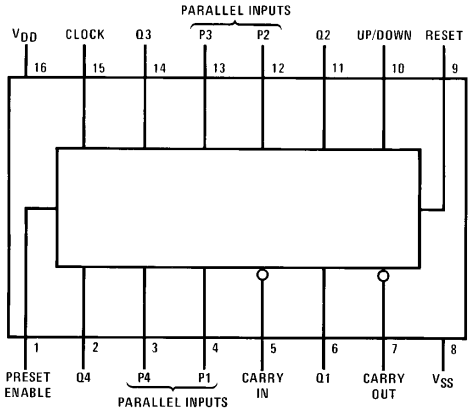
All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- Parallel load "jam" inputs
- Low quiescent power dissipation — 0.25 μW/package (typ.) @ $V_{CC}=5.0V$
- Motorola MC14510, MC14516 second source

Connection Diagram

Dual-In-Line Package



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Top View

Order Number CD4510B or CD4516B

Truth Table

Clock	Reset	Preset Enable	Carry In	Up/Down	Output Function
X	1	X	X	X	Reset to Zero
X	0	1	X	X	Set to P1, P2, P3, P4
⌐	0	0	0	1	Count Up
⌐	0	0	0	0	Count Down
¬	0	0	X	X	No Change
X	0	0	1	X	No Change

⌐ = Positive Transition
¬ = Negative Transition
X = Don't Care

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temp. (T_L) (Soldering, 10 sec.)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range	
CD4510BM, CD4516BM	−55°C to +125°C
CD4510BC, CD4516BC	−40°C to +85°C

DC Electrical Characteristics CD4510BM/CD4516BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.05	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.1	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.15	20		600	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.8		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.0		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.8		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.0		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−7.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4510BC/CD4516BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.05	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.1	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.15	80		600	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4510BC/CD4516BC (Note 2) (Continued)

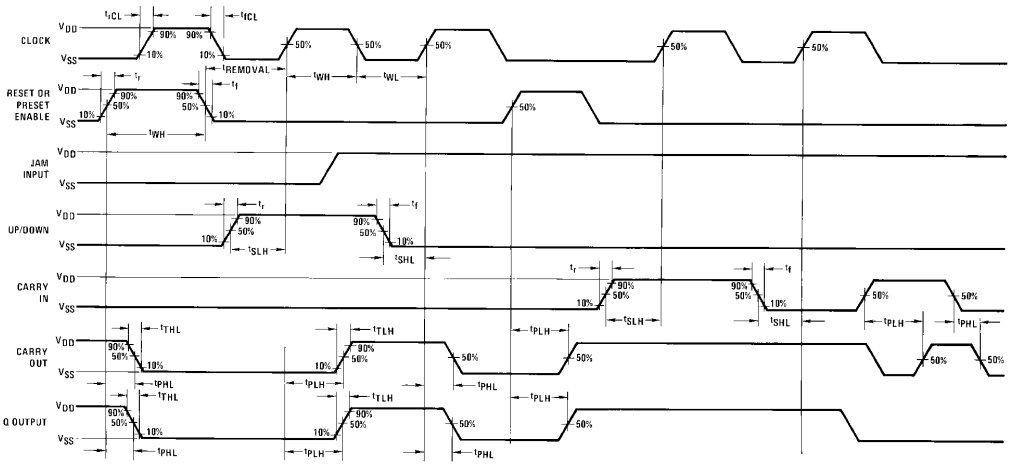
Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.8		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.0		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.8		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.0		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−7.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Switching Time Waveforms



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AC Electrical Characteristics* CD4510BM/CD4510BC, CD4516BM/CD4516BC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_{rCL} = t_{fCL} = t_r = t_f = 20$ ns, unless otherwise specified

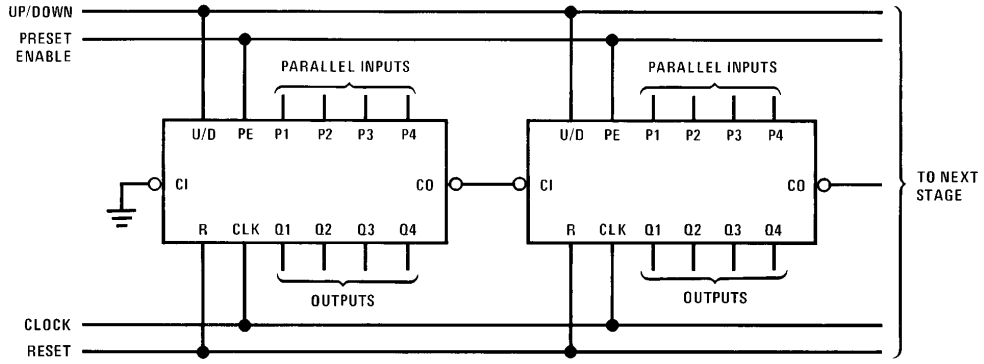
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q Outputs	$V_{DD} = 5V$		220	500	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Carry Output	$V_{DD} = 5V$		315	630	ns
		$V_{DD} = 10V$		130	260	ns
		$V_{DD} = 15V$		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q and Carry Outputs	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		160	315	ns
		$V_{DD} = 10V$		65	130	ns
		$V_{DD} = 15V$		50	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	15			μs
		$V_{DD} = 15V$	15			μs
t_{SU}	Minimum Carry In Setup Time	$V_{DD} = 5V$		100	220	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		35	70	ns
t_{SU}	Minimum Up/Down Setup Time	$V_{DD} = 5V$		200	420	ns
		$V_{DD} = 10V$		70	170	ns
		$V_{DD} = 15V$		60	150	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	3.1		MHz
		$V_{DD} = 10V$	3.8	7.6		MHz
		$V_{DD} = 15V$	5.0	10.0		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)	Per Package		65		pF
RESET/PRESET ENABLE OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Q Output	$V_{DD} = 5V$		285	570	ns
		$V_{DD} = 10V$		115	230	ns
		$V_{DD} = 15V$		95	195	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Carry Output	$V_{DD} = 5V$		420	860	ns
		$V_{DD} = 10V$		170	350	ns
		$V_{DD} = 15V$		140	290	ns
t_{WH}	Minimum Reset/Preset Enable Pulse Width	$V_{DD} = 5V$		90	200	ns
		$V_{DD} = 10V$		40	100	ns
		$V_{DD} = 15V$		35	80	ns
t_{REM}	Minimum Reset/Preset Enable Removal Time	$V_{DD} = 5V$		170	330	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		60	120	ns
CARRY INPUT OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry In to Carry Output	$V_{DD} = 5V$		260	500	ns
		$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		90	180	ns

*AC Parameters are guaranteed by DC correlated testing.

Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L) V_{DD}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; P_Q = Quiescent Power Dissipation. For further details, see application note AN-90, "54C/74C Family characteristics".

Cascading Packages

Parallel Clocking



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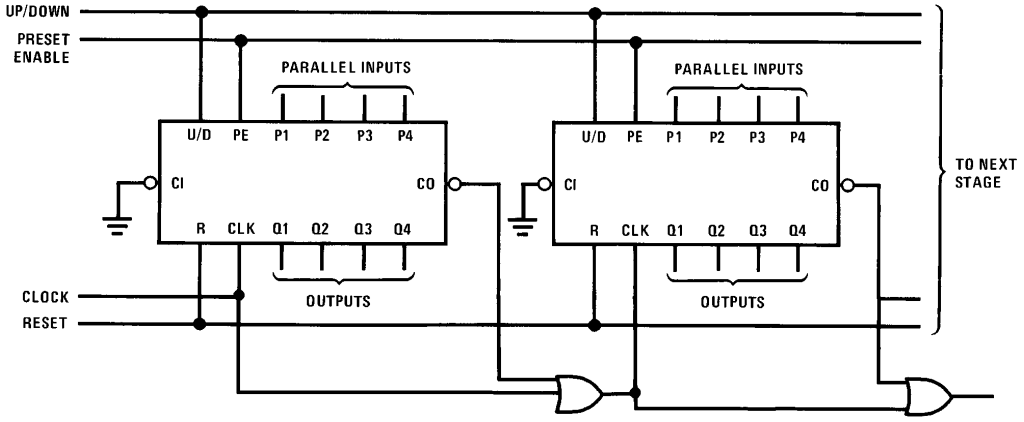
Ripple Clocking



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Schematic Diagrams

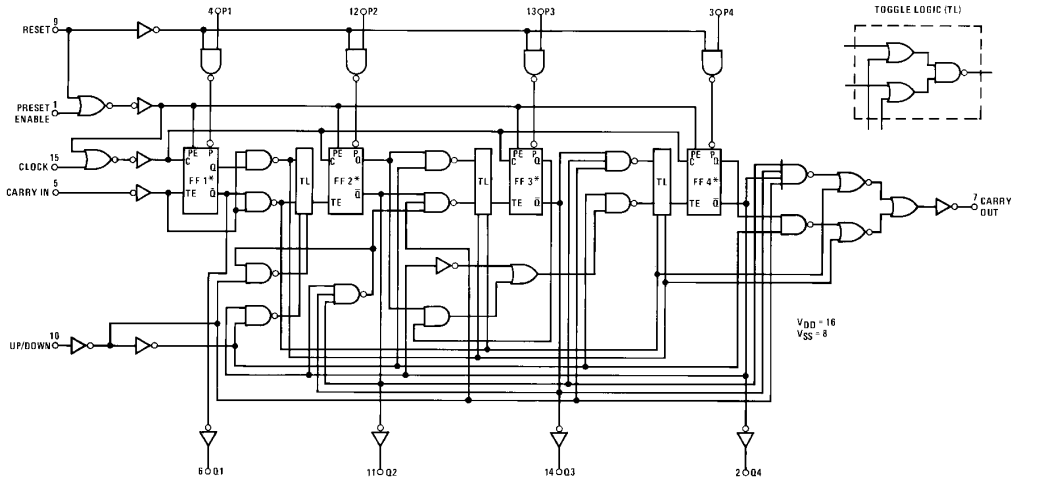

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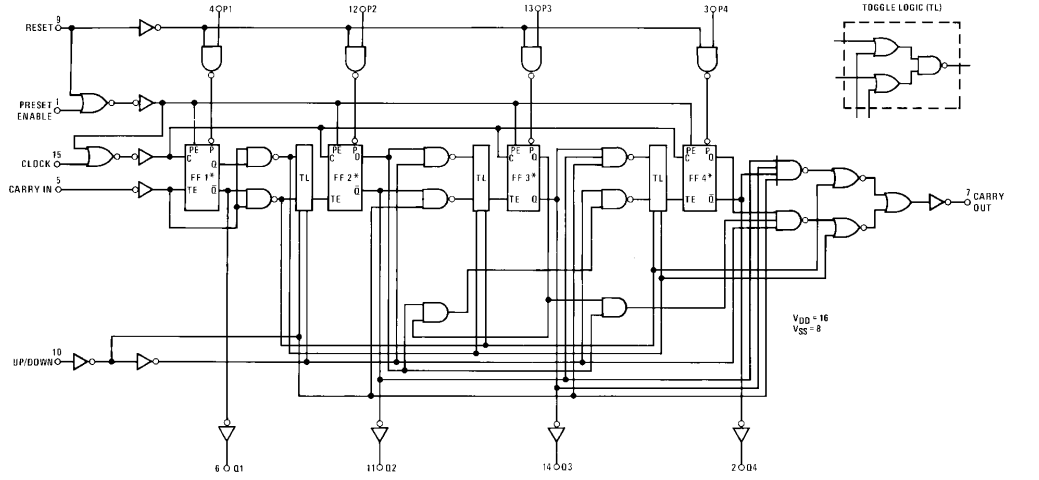
FIGURE 1. CD4510



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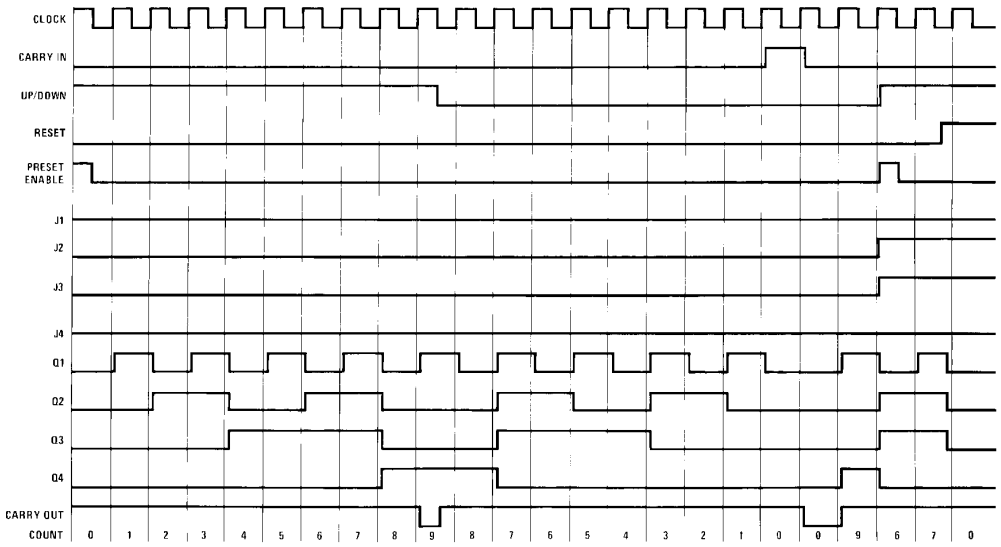
*Flip-flop toggles at the positive-going edge of clock (C) if Toggle Enable (TE) is at logical ''1'' and Preset Enable (PE) is at logical ''0''

FIGURE 2. CD4516

Logic Waveforms

CD4510BM/CD4510BC



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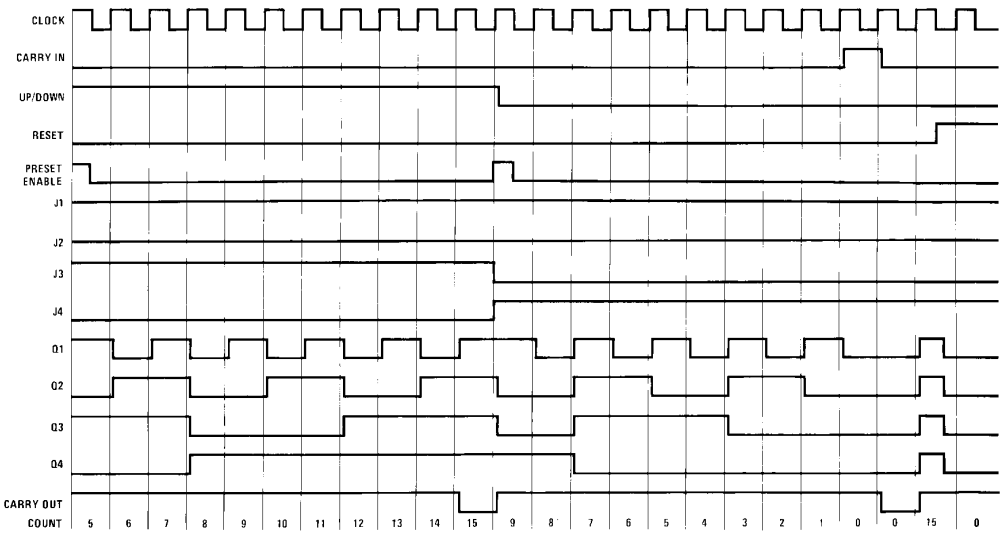
CD4516BM/CD4516BC



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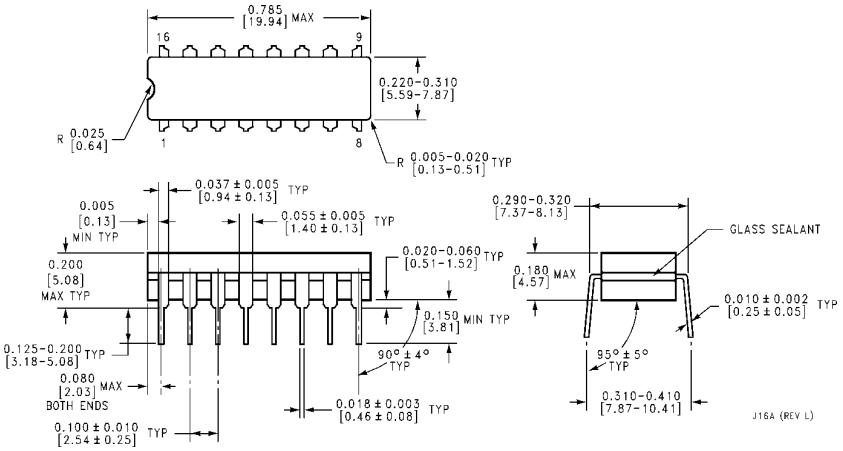
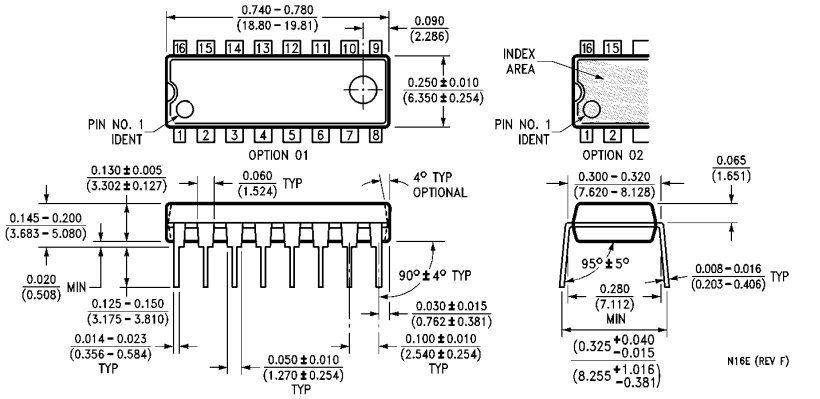
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4510BMJ, CD4510BCJ, CD4516BMJ or CD4516BCJ
NS Package Number J16A



Molded Dual-In-Line Package (N)
Order Number CD4510BMN, CD4510BCN, CD4516BMN or CD4516BCN
NS Package Number N16E

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